## AMENDMENTS TO THE SPECIFICATION

*Please amend the paragraph beginning on page 3, line 24 as follows:*

However, the motherboard has a large variation in the shrinkage rate in firing. The spacings between dicing lines ~~are deviated~~ deviate from the corresponding conductive patterns arranged on the motherboard to be cut. Accordingly, as the distance between the dicing line and the reference point of the motherboard is longer, the deviation from the corresponding conductive pattern on the motherboard is larger. For example, when the motherboard is cut using one end thereof as the reference point, the variation in shrinkage of the motherboard significantly affects the dicing line in the vicinity of the other end. In addition, as the difference between the shrinkage rate of the motherboard in firing and a set value becomes larger, the deviation becomes more pronounced.

*Please amend the paragraph beginning on page 5, line 2 as follows:*

The present invention provides a line transition including a solid waveguide and a planar circuit to realize a planar-circuit to waveguide transition, the solid waveguide propagating electromagnetic waves within a three-dimensional space, the planar circuit being constructed by forming a predetermined conductive pattern on a dielectric substrate, wherein the dielectric substrate is disposed parallel to the E plane of the solid waveguide in almost the middle of the solid waveguide, the conductive pattern on the dielectric substrate includes a coupled-line pattern segment electromagnetically coupled with a signal propagating through the solid waveguide and a transmission-line pattern segment extending from the coupled-line pattern segment. The edge of the dielectric substrate has a notch in the vicinity of the coupled-line pattern segment, the notch having a side that is parallel to the signal propagation direction of the coupled-

line pattern segment, the length of the side being equal to or longer than the dimension in the width direction of the E plane of the solid waveguide.

*Please amend the paragraph beginning on page 8, line 5 as follows:*

A line transition according to a first embodiment and a method for manufacturing the line transition will now be described with reference to Figs. 1A-1C, 2A-2C, 3 and ~~to~~ 4.

*Please amend the paragraph beginning on page 8, line 8 as follows:*

Figs. 1A through 1C show the structure of a dielectric substrate serving as a component of the line transition. Fig. 1A is a top view of the dielectric substrate, Fig. 1B is a bottom view thereof, and Fig. 1C is an enlarged view of a portion shown by a broken line in Fig. 1B. On the upper surface of a dielectric substrate 3, a ground conductor 21, chip connection electrodes 22, 23, 24, 25, 26 ~~22 to 26~~, and external connection terminals 27, 28, 29 ~~27 to 29~~ are formed (Fig. 1A). Terminals of a chip 8 are soldered to the chip connection electrodes 22, 23, 24, 25, 26 ~~22 to 26~~, respectively.

*Please amend the paragraph beginning on page 8, line 23 as follows:*

A notch N1 is formed at one edge of the dielectric substrate 3 in the vicinity of the coupled-line conductor 14k. Similarly, as shown in Fig. 1B, a notch N2 is formed at another edge of the dielectric substrate 3 in the vicinity of the other coupled-line conductor 15k. The notch N1 has a side E1 that is parallel to the signal propagation direction of the coupled-line conductor 14k. The notch N2 has a side E2 that is parallel to the signal propagation direction of the coupled-line conductor 15k.

*Please amend the paragraph beginning on page 9, line 7 as follows:*

The end of the ground conductor 11 is arranged in the vicinity of the coupled-line conductor 14k. A plurality of via holes V (Fig. 1C) for electrically coupling the upper and lower ground conductors 11 and 21 on the dielectric substrate 3 are formed in this edge of the ground conductor 11. Similarly, another edge of the ground conductor 11 is disposed in the vicinity of the coupled-line conductor 15k. A plurality of via holes for electrically coupling the upper and lower ground conductors 11 and 21 are formed in this edge.

*Please amend the paragraph beginning on page 10, line 14 as follows:*

A plane ES (Fig. 2C) that is parallel to each of the lower and upper conductive plates 1 and 2 of the waveguide corresponds to the E plane that is parallel to the electric field in the TE10 mode serving as an electromagnetic-wave propagating mode. In this manner, the dielectric substrate 3 is arranged parallel to the E plane in almost the middle of the waveguide.

*Please amend the paragraph beginning on page 10, line 21 as follows:*

The sides E1 and E2 of the respective notches N1 and N2 shown in FIG. 1B are parallel to the coupled-line pattern segments 14k and 15k, respectively. The length of each of the sides E1 and E2 is equal to or longer than the dimension in the width direction of the E plane ES.

*Please amend the paragraph beginning on page 11, line 1 as follows:*

As shown in Figs. 1A and 1B, the ground electrode 21 is not formed (a space A1, A2 is provided) on the rear surface (upper surface of the dielectric substrate 3) of the

portion where the coupled-line conductors 14k and 15k ~~is~~ are formed, the surface facing the lower conductive plate 1. ~~This space functions~~ These spaces function as a suspended line. The suspended line is electromagnetically coupled with the propagating mode of the waveguide including the dielectric strips 6 and 7 and the conductive plates 1 and 2.

*Please amend the paragraph beginning on page 12, line 3 as follows:*

A signal supplied from the external connection terminal 27 shown in Fig. 1A is propagated to the connection conductor 24 through the transmission-line conductor 16 as shown in Fig. 1B. According to the present embodiment, the chip 8 in Fig. 1A and Fig. 6 includes a x2 multiplier MLT, amplifiers AMPa and AMPb, a directional coupler CPL, and an amplifier AMPc.

*Please amend the paragraph beginning on page 13, line 9 as follows:*

Fig. 4 shows a motherboard to be cut into dielectric substrates 3. In Fig. 4, broken lines VL0, VL1', VL1, VL2', VL2, VL3', VL3, ~~to~~ VL4' and HL0, HL1, HL1;, HL2, HL2', HL3, HL3', ~~to~~ HL4 indicate dicing lines of a motherboard 30. The conductive pattern shown in Fig. 1A is formed on each of workpieces obtained by cutting the motherboard along the vertical and horizontal dicing lines. Through holes H1 and H2 are formed between each workpiece and adjacent workpieces. Referring to Fig. 4, the dicing line VL3 passes through the through hole H1 formed between a right upper dielectric-substrate workpiece 3' and the adjacent dielectric-substrate workpiece on the left. The dicing line HL1 passes through the through hole H2 between the dielectric-substrate workpiece 3' and the adjacent lower dielectric-substrate workpiece.

*Please amend the paragraph beginning on page 14, line 21 as follows:*

As shown in FIG. 4, using the vertical and horizontal dicing lines VL0, VL1', VL1, VL2', VL2, VL3', VL3, ~~to~~ VL4' and HL0, HL1, HL1;, HL2, HL2', HL3, HL3', ~~to~~ HL4, the motherboard 30 is cut into individual dielectric substrates 3.

*Please amend the paragraph beginning on page 15, line 9 as follows:*

w: 3.0 (Fig. 1C)

*Please amend the paragraph beginning on page 15, line 10 as follows:*

db: 0.5 (Fig. 1C)

*Please amend the paragraph beginning on page 15, line 11 as follows:*

da: 0.6 (Fig. 1C)

*Please amend the paragraph beginning on page 15, line 12 as follows:*

L: 0.2 (Fig. 1C)

*Please amend the paragraph beginning on page 15, line 13 as follows:*

t: 0.2 (Fig. 2B)

*Please amend the paragraph beginning on page 15, line 14 as follows:*

Hd: 1.8 (Fig. 2B)

*Please amend the paragraph beginning on page 15, line 15 as follows:*

wg~~Wg~~: 1.2 (Fig. 2A)

*Please amend the paragraph beginning on page 15, line 16 as follows:*

wd~~Wd~~: 1.1 (Fig. 2A)

*Please amend the paragraph beginning on page 15, line 17 as follows:*

R: 0.5R (Fig. 1C),